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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,811	02/25/2005	Katarzyna Leijten-Nowak	NL02 0823 US	1165

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PHILIPS ELECTRONICS NORTH AMERICA CORPORATION
INTELLECTUAL PROPERTY & STANDARDS
1109 MCKAY DRIVE, M/S-41SJ
SAN JOSE, CA 95131

EXAMINER

WENDLER, ERIC J

ART UNIT PAPER NUMBER

2824

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

613

Office Action Summary	Application No. 10/525,811	Applicant(s) LEIJTEN-NOWAK, KATARZYNA	
	Examiner Eric Wendler	Art Unit 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 9/1/06.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2 and 4-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-2, 4-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 February 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is responsive to the following communications: the Application filed on February 25, 2005.
2. Claims 1-2, 4-9 are pending in the present application. Claim 1 is an independent claim.

Specification

3. The disclosure is objected to because of the following informalities: the proper sections of the specification must be denoted by titles such as "Background of the Invention", "Summary of the Invention", "Brief Descriptions of the Drawings", and "Detailed Description of the Preferred Embodiments".

Appropriate correction is required.

Response to Arguments

4. Applicant's arguments filed September 1, 2006, have been fully considered but they are not persuasive. The new material added to claim 1, which was previously presented as claim 3, refers to a device in which a read operation is performed in a first phase of a control signal, and a write operation is performed in a second phase of a control signal. A device in which a read operation is performed on a rising edge, or first phase, of a clock signal, and a write operation is performed on a falling edge, or second phase, of a clock signal, would read on these claimed limitations since the clock signal is essentially a control signal that controls these operations. Yamada teaches, in column 6, lines 8-10, that a RAM that performs a writing operation at the trailing edge of a clock signal (inherently meaning that the read operation is performed on the rising

edge of the clock signal) can be employed in his shift register system. The rejection of the claimed subject matter is therefore maintained.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent to Yamada (4,393,482).**

7. **Regarding claim 1**, Yamada teaches data storage elements (RAM) for storing at least two data elements, a decoder **29** having an output connected to the data storage elements for accessing the data storage elements, and an address generator comprising a modulo-N counter **23** for generating the bit pattern (column 7, lines 15-34; Fig. 9). Yamada also teaches the RAM can be of a synchronous or non-synchronous type, in which case the read operation can be performed in a first phase of a control or timing signal, and a write operation can be performed in a second phase of a control or timing signal (column 5, lines 59-68; column 6, lines 1-10).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Yamada (4,393,482) in view of the US Patent to Bauer (5,889,413).

10. Regarding claim 2, Yamada teaches all the claimed elements as discussed above but fails to explicitly teach that the device comprises a look-up table being operable as the collection of data storage elements. Bauer teaches a logic element which can be configured as any one of a RAM, a shift register, and a look-up table. It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the teachings of Yamada with the teachings of Bauer since the device of Bauer can provides additional advantages brought about by the possibility of acting as a shift register, or a look-up table, as well as acting as the RAM in the system of Yamada.

11. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Yamada (4,393,482).

12. Regarding claims 5-7, Yamada discloses the claimed invention except for additional collections of data storage elements and their respective controllers. It would have been obvious to one of ordinary skill in the art, at the time the invention was made to implement additional collections of data storage elements and their respective controllers in order to increase storage space, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

St. Regis Paper Co. v. Bernis Co., 193 USPQ 8.

13. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Yamada (4,393,482) in view of the US Patent to Keating (5,404,170).

14. **Regarding claims 5-7**, Yamada discloses the claimed invention except for additional collections of data storage elements and their respective controllers. Keating teaches multiplexers that act as controllers in accessing multiple video stores in a system that is similar to that of Yamada. It would have been obvious to one of ordinary skill in the art, at the time the invention was made to combine the teachings of Keating with those of Yamada to allow the system of Yamada to access multiple collections of memory controlled by multiplexers or similar circuitry (demultiplexers, etc.).

15. **Claims 4, 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Yamada (4,393,482) in view of the US Patent to Shinohara et al. (5,177,706).**

16. **Regarding claim 4**, Yamada teaches all the claimed elements as discussed above but fails to explicitly teach a configurable switch coupled between a memory element and a data input, which is conductive during a part of a second phase of a control signal. Shinohara et al. teach such a switch used with a similar type of memory (column 7, lines 1-13). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use the switch of Shinohara et al. with the memory system of Yamada since they both teach similar types of memories and the use of such switches is well known in the art.

17. **Regarding claims 8-9**, Yamada teaches all the claimed elements as discussed above but fails to explicitly teach that the selection signals are derived from the most significant bits of the bit patterns, and that the control circuitry comprises a configuration network for configuring the size of the data storage device. Shinohara et al. teach both

Art Unit: 2824

these limitations (column 6, line 40 - column 8, line 61; column 11, line 31 - column 12, line 44). It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the teachings of Yamada and Shinohara et al. since deriving selection signals from the most significant bits of bit patterns is well-known in the art, and a configuration network such as that taught by Shinohara et al. would allow the system of Yamada to function easily and more efficiently should multiple collections of data storage devices be used.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

Art Unit: 2824

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJW
11/7/06

Anh Phung 11/11/06

**ANH PHUNG
PRIMARY EXAMINER**